AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Please amend the third paragraph on page 9 as follows:

According to the present invention, there is provided a semiconductor device, comprising: an insulating resin layer; and a semiconductor chip mounted on said insulating layer; wherein said insulating resin layer includes a patterned interconnect line embedded therein, and wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.

Please amend the last paragraph on page 9 and continuing onto page 10 as follows:

According to the present invention, there is provided a method for manufacturing a semiconductor device, comprising: providing a semiconductor device-forming region on a surface of a substrate; forming a layer structure in said semiconductor device-forming region on said substrate, said layer structure including an insulating resin layer and a patterned interconnect line being embedded in said insulating resin layer; mounting a semiconductor chip on said layer structure, respectively; molding said semiconductor chip with an insulating material in said semiconductor device-forming region□ removing said substrate; exposing at least a part of said patterned interconnect line; and dicing said insulating resin outside said semiconductor device-forming region and separating thereof into a module-forming unit to form a semiconductor device, wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.

Please amend the first full paragraph on page 10 as follows:

According to the present invention, there is provided a thin plate interconnect line member having a semiconductor chip-mounting surface and an interconnect line substrate-coupling surface opposite to said chip-mounting surface, comprising: an insulating resin layer; and a patterned interconnect line being embedded within said insulating resin layer, wherein at least a part of said patterned interconnect line is exposed on said interconnect line substrate-coupling surface, and wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.

Please amend the first paragraph on page 20 as follows:

Furthermore, although the interlayer insulating film 405 may be constituted by a material that substantially expands or shrinks by treating heat, the interlayer insulating film 405 is preferably constituted by a material having the coefficient of thermal expansion within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~. By using the material having the coefficient of thermal expansion (ppm/degree centigrade) of the above range to manufacture a semiconductor device, influence of variety of heat hysteresises that are burden to the semiconductor device during the manufacturing process thereof can be reduced. Thus, displacement of alignment of layers composing the semiconductor device is reduced. As a result, the semiconductor device having improved high frequency performance can be obtained.